

W&B Ref. No.: INF 2067-US Attorney Docket No.: INFN/WB0042

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nikolaus Brüls

Serial No.: 10/723,292

Confirmation No.: 5561

Filed:

November 26, 2003

For: VITERBI DECODER

Mail Stop AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

 $oldsymbol{\omega}$ Group Art Unit: 2127

Examiner:

unknown

CERTIFICATE OF MAILING 37 CFR 1.8

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While the information submitted in this Information Disclosure Statement may be material pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to therein is prior art for this invention unless specifically designated as such.

PATENT

W&B Ref. No.: INF 2067-US Attorney Docket No.: INFN/WB0042

In accordance with 37 CFR § 1.97, this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possibly material information as defined under 37 CFR § 1.56(a) exists.

The patents and/or publications submitted herewith are set forth on the attached Form PTO-1449.

If the sum of \$180.00 is due under 37 CFR § 1.17(p) pursuant to § 1.97, the Commissioner is hereby authorized to charge this fee, and any other fee necessary to make this submission timely, to the Deposit Account No. 20-0782/INFN/WB0042/GGM.

Respectfully submitted,

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Sheet 1 of 1

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Application Number	10/723,292
Filing Date	November 26, 2003
First Named Inventor	Nikolaus Brüls
Group Art Unit	2127
Examiner Name	Unknown
Attorney Docket Number	INFN/WB0042
Submission Date	March 8, 2005

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²	
. ,	C1	G.D. FORNEY, JR., "The Viterbi Algorithm"; Proc. IEEE, Vol. 61, No. 3, March 1973, pp. 268-278.		
	C2	PETER J. BLACK et al. "A 140-Mb/s, 32-state, Radix-4 Viterbi Decoder"; IEEE Journal OF Solid-State Circuits, Vol. 27, No. 12, December 1992, pp. 1877-1885.		
	C3	GERHARD FETTWEIS et al. "A 100 Mbit/s Viterbi Decoder Chip: Novel Architecture and its Realization"; Proc. IEEE ICC, Vol. 2, Atlanta August 1990, pp. 463-467.		
_	C4	ALFRED K. YEUNG et al. "A 210Mb/s Radix-4 Bit-level Pipelined Viterbi Decoder", 1995 IEEE International Solid-State Circuits Conference, pp. 88-89, 304.		
	C5	V.S. GIERENZ et al. "A 550 Mb/s Radix-4 Bit-Level Pipelined 16-State 0.25-µm CMOS Viterbi Decoder"; Proc. IEEE Inter.Conf. on Application-Specific Systems, Architectures, and Processors; Boston, July 2001, pp. 195-201.		
	C6	R. H. KRAMBECK et al. "High-Speed Compact Circuits with CMOS"; IEEE Journal OF Solid-State Circuits, Vol.SC-17, No. 3, June 1982, pp. 614-619.		
	C7	German Patent Office Decision to Grant dated September 30, 2003.		
	C8			

Examiner Date Considered

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